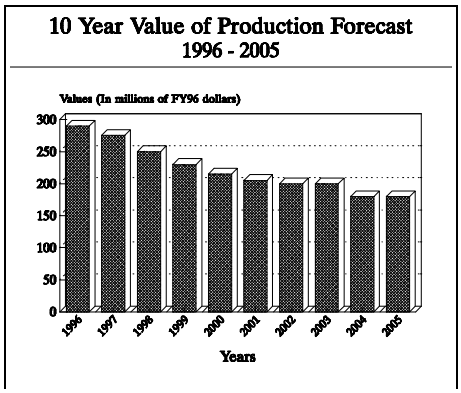
VHSIC - Archived 3/97

Outlook

- Evolves technology inserts for other programs
- Applications mushrooming



Orientation

Description. The Very High Speed Integrated Circuit (VHSIC) program is the US DoD initiative to develop advanced silicon integrated circuit technology.

Sponsor

Under Secretary of Defense for Research & Engineering

VHSIC Program Office

(Program manager and overall director)

The following agencies monitor work:

Department of Defense

Advanced Research Projects Agency (ARPA)

Arlington, VA

US Air Force

Air Force Aeronautical Laboratories

Wright-Patterson AFB, OH

Rome Air Development Center (RADC)

Griffiss AFB, NY

US Army

Armament Research and Development Command (ARDC)

Dover, NJ

Communications & Electronics Command

Ft. Monmouth, NJ

Electronic Technology and Device Laboratories

Ft. Monmouth, NJ

Electronic Warfare Laboratory

Ft. Monmouth, NJ

Missile Command (MICOM)

Huntsville, AL

Center for Night Vision and Electro-Optics

Ft. Belvoir, VA

Army Research Office (ARO)

Research Triangle Park, NC

US Navy

Naval Air Development Center (NADC)

Warminster, PA

Naval Ocean Systems Center (NOSC)

San Diego, CA

Naval Research Laboratory (NRL)

Washington, DC

Naval Surface Weapons Center (NSWC)
Dahlgren, VA, and White Oak, MD
Naval Weapons Center (NWC)
China Lake, CA
Office of Naval Research (ONR)
Arlington, VA
Space and Naval Warfare Command (SPAWAR)
Washington, DC

Contractors

AT&T
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Electronic Systems Group

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Status. The program has come to a successful conclusion. VHSIC technology and development have matured to a level that they are now infused in recipient programs. The program served as the model for the formulation of the Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC) program which has been similarly successfully concluded and replaced by the current Microwave and Analog Front End Technology (MAFET) initiative.

Total Produced. Processor modules with VHSIC chips are currently being produced and installed in a broad spectrum of military and commercial systems.

Application. The goal of the VHSIC program was to correct deficiencies in DoD integrated circuit technology in order to provide system developers and acquisition managers with a military qualified diverse microelectronics technology base that was as an improvement over then available commercial technology.

Price Range. Indeterminate due to the developmental nature of the program.

Technical Data

Design Features. VHSIC was a tri-service effort, centrally managed by the Office of the Under Secretary of Defense for Research and Engineering (USDRE) and funded in the Air Force budget. The VHSIC program has involved production of prototype integrated circuits, brassboard demonstration subsystems, pilot production lines, computer-aided design tools and device technology.

Initial VHSIC applications included digital signal processors for radar, ASW, communications, missile guidance, electronic warfare and optical sensor systems. VHSIC was expected to enhance the performance and reliability of these systems, as well as reducing overall cost. The ALQ-l3l EW jamming pod and the UYS-1 Acoustic Signal Processor were the first systems to be the recipients of VHSIC chips.

Additional efforts in the program included military qualification and yield enhancement of the Phase 1 chips, development of design automation tools to accelerate the design of advanced military systems using VHSIC level technology, and development of key lithographic tools for chip manufacture such as deep ultra-violet, electron beam and x-ray technologies. The program also provided for rapid and early demonstrations of the Phase 1 technology through the technology insertion program.

The following phases and distinct activities have been associated with the program, starting in 1980:

Phase 0. — This initial phase of the program was used to define VHSIC technical concepts and prepare a detailed development plan. The emphasis was on achieving a 1.25 micron minimum feature size and 25 megahertz clock speed.

Phase 1. — This phase was directed to the successful development and production of silicon chips with a characteristic 1.25 micron minimum feature size and 25 MHz clock speed, and to their demonstration in system brassboards. Phase 1 later was expanded to include a yield enhancement program to increase the yield, i.e. producibility of VHSIC chips.

Phase 2. — Primary emphasis was on the development and production of silicon chips with a 0.5 micron minimum feature size and 100 MHz clock speed. The effort was begun after it became evident that development of the 1.25 micron technology and its transition into manufacturable products could, in fact, be accomplished.

Phase 3. — his initiative involved a broad-based collection of separately funded contracts conducted concurrently with Phases 1 and 2 which were found to be necessary to support overall program objectives. Specific work items included technology applications, materials requirements, lithography and fabrication tools, design software development, packaging, chip qualification, and radiation hardness developments.

Manufacturing Technology. — Better manufacturing tools and techniques needed to make VHSIC chips producible and affordable were developed in this effort.

Design Automation. — This effort covered the development of the design tools, standards, software, and hardware needed to make the design of large, complex VHSIC chips more effective and affordable.

Technology Insertion. — This effort undertook the demonstration of VHSIC Phase 1 technology chips by inserting them into a wide variety of military systems, both existing designs and those then in development.

Variants/Upgrades

Development of VHSIC components is a constantly evolving process. Although there will be no more new starts under the formal structure of the VHSIC program, development will continue as part of the work conducted in the development new military and commercial electronics based systems. Continued development will be driven by cost reduction and continuing technical objectives to further reduce equipment size and increase system complexity.

Program Review

Background. During the late 1970s, US Government concern over the erosion of the US lead in high technology was heightened by reports from intelligence agencies that the Soviet military had succeeded in incorporating US commercial integrated circuit designs into some of its weapon systems faster than the Pentagon was able to accomplish this same task with its systems. This led to the creation of the VHSIC program, and the reaffirmation of DoD's policy to use technology to overcome numerical superiority on the battlefield.

Phase 0 feasibility contracts for the VHSIC program were awarded in March 1980 to Hughes, Rockwell, GE, TRW, IBM, Westinghouse, TI, Honeywell, and Raytheon. Phase 1 contracts were subsequently awarded in May 1981 to Hughes, TI, IBM, TRW, Honeywell and Westinghouse for development of first generation Very Large Scale Integrated (VLSI) components. By FY82, the Air Force had reported substantial progress on defining chip fabrication processes, developing and integrating computer-aided design tools and completing initial chip designs. Also in FY82, results from Phase 3 efforts in high resolution lithography and fault tolerant design techniques were incorporated into Phase 1, and requirements for Phase 2 chip designs were established. Work continued on Phase 1 chip designs and processing schedules in FY83. Work also began that year on a VHSIC hardware description language to speed integration of Phase 1 efforts into operational systems.

DoD awarded nine contracts, valued at approximately US$1 million each, in August 1983 for design studies of submicron VHSIC geometries. In November 1983, the first of the new Phase II VHSIC contractor teams was identified, as were the responsibilities of its team members. The team was to be headed by Western Electric, with team members to include Bell Labs and E-Systems' Melpar Division. Western Electric was responsible for chip production, Bell Labs for chip design and process technology, and E-Systems for systems applications. The other two new VHSIC teams were headed by Harris Corp and RCA.

Phase 2 contracts, awarded in FY84 for the development of submicrometer pilot lines and second-generation brassboards, continued in FY85. The effort focused on the demonstration of a standard production process and definition of brassboard specifications. The Phase 1 yield enhancement thrust supported a wide range of trouble shooting efforts, aimed at the resolution of various Phase 1 pilot line production problems. The initial VHSIC hardware descriptive language (VHDL) tools were delivered, and the IDAS effort continued. Phase 1 chips became available in sufficient quantities to permit prototyping and evaluation.

The Phase 1 yield enhancement thrust was completed in late FY86. The VHDL Analyzer and Design Library Manager were also delivered. Testing of the VHDL by various government and industrial organizations was started in FY86. Design reviews on the Tester Independent Support Software System (TISSS) were completed. The Phase 2 contractors demonstrated working 0.5 micrometer circuits on test chips and completed design of a proof of concept 0.5 micron chip and interoperability standards. The first use of VHSIC technology in two operational weapon systems (the ALQ-131 electronic countermeasures pod and UYS-1 Acoustic Signal Processor) was successfully demonstrated in FY86. The VHSIC chip tester, installed at the Rome Air Development Center, was brought up to operational capability in FY86, and was subsequently made available for testing VHSIC chips produced by commercial sources.

In FY87 Phase 2 contractors completed process development and fabrication of a Bus Interface chip and associated proof of concept demonstration. Phase 2 contractors continued the design of brassboard modules and started design on additional Phase 2 chips. The qualification program continued in FY87 in two phases. In the first phase, a representative chip from each contractor was subjected to established military standard qualification requirements. This tested the basic integrity of each supplier's process and design system. Five representative chips were expected to complete this qualification process in FY87. The second phase of the qualification program was aimed at assuring potential users that all members of a chip set are (and will continue to be) equally suited for insertion into military systems. This step required revision to several — then current military standards.

Also in FY87, development continued on the Tester Independent Support Software System (TISSS) effort with coding of the software. The VHSIC hardware description language program was scheduled to be completed and an Institute for Electrical and Electronic Engineer Industry standard based on VHDL finished. Work was initiated to establish a pilot production line using the latest state-of-the-art X-ray lithography. This effort was necessary to help establish manufacturing experience in using X-ray lithography to develop 0.5 micron circuits.

In FY88, submicron technology development continued, with Phase 2 contractors designing and developing additional VHSIC chips incorporating 0.5 micron features. These chips were integrated into brassboard modules for evaluation. Phase 2 technology was identified as offering the significant advances in system performance, reliability, size, weight and power requirements needed by military system designers to develop next generation equipment. Final demonstration and testing of the TISSS was completed and made available for use by the government and commercial industry. Efforts continue on the development of a pilot production line using X-ray lithography equipment. Definition of the VHSIC Engineering Information System (VEIS) was completed and implemented. Work on the development of system level design automation tools was also completed.

In FY89 development of VHSIC submicron technology was completed with delivery of chips and brassboard modules for test and evaluation. By this point in the program, Phase 2 contractors were to have put as many as 20 million transistors with 0.5 micron dimensions on a single chip. Work on developing and demonstrating a pilot line using X-ray lithography was completed. The Engineering Information System prototype was delivered. Radiation enhancement work for Phase 2 submicrometer circuits and in-house test and evaluation of VHSIC chips were completed. Early demonstration programs emphasizing the rapid insertion of VHSIC technology were completed. Demonstrations conducted under this early insertion thrust included signal processors for radar, electronic warfare and communications applications. The testing and verification of generic qualification procedures were also completed.

In 1990, the VHSIC Phase 2 contractor team of TRW/Motorola announced development of the Central Processing Unit — Advanced Extended (CPUAX) superchip containing approximately four million 0.5µ devices and capable of performing 200 MFLOPS. The fully packaged chip contains spare components on the surface chip, developed by TRW, that allows for self repair. The complete chip measures 53 mm square and weighs 42 g. This superchip is designed to operate as the "brain" of advanced digital processing systems used in a range of air, ground, and spaced-based systems including advanced spacecraft, aircraft and missiles.

As of early 1995, VHSIC devices are being put into production in various US programs and equipments wherever high speed computer processing is needed. Other countries are beginning to follow the US lead in this microelectronics field with government sponsored development programs of their own. The British and French governments have initiated the VHPIC (Very High Performance Integrated Circuity) and CITGV programs, respectively, paralleling the VHSIC effort.

System Insertion Breakout. The following systems are to be, or have been, tested with VHSIC components, or are candidates for VHSIC insertion. They are all systems that were formally planned and jointly funded by the VHSIC Program Office and the corresponding System Program Offices.

Army

Enhanced PLRS (EPLRS) User Unit

Light Helicopter Family (LH) Mission Computer

TOW Missile Automatic Target Tracker

Firefinder Radars (TPQ-36/37)

Common Module VHSIC Integrated System: part of Armored Forces Modernization effort

Miniaturized ESM/ELINT Direction Finding & Location Intercept (MEDFLI) signal processor

Hellfire Missile Imaging Infrared Seeker

Multi-role Survivable Radar (MRSR)

Army Command and Control System (ACCS)

MLQ-34 TACJAM EW system

Navy

UYS-2 Enhanced Modular Signal Processor (EMSP)

MK-50 Advanced Lightweight ASW Torpedo

HF/EHF Communications; VHSIC Terminal Brassboard (VTB)

AYK-14(V) Standard Airborne Computer VHSIC Processor Module (VPM)

Advanced ASW Receiver

VHSIC Communications Processor (VCP)

SRS-1 Combat Direction Finder

SLQ-32 EW suite

Tactical Air Operations Module (joint Air Force/ Marines)

Air Force

ALQ-131 Electronic Countermeasures Pod

Advanced Spacecraft Computer Module (ASCM)

Cruise Missile Advanced Guidance

Common Signal Processor (CSP)

MILSTAR Terminal/Modem Processor

E-3A Signal Processor

F-15 VHSIC Central Computer (VCC)

Radiation Hard 32-bit Processor (RH32)

Generic VHSIC Spaceborne Computer (GVSC)

Advanced Onboard Signal Processor Radiation Hardened Vector Processor (RHVP)

APG-68 Radar Advanced Programmable Signal Processor (APSP)

ATF Processing

SRAM II Missile Guidance Computer

Tactical Air Operations Module (joint Air Force/ Marines)

VHSIC Avionics Modular Processor (VAMP)

The following systems are independent insertion projects, some of which were IRAD funded. Others were funded by a particular service.

AT&T. UYS-2 EMSP (Navy)

General Dynamics. M1A2 tank power and data bus controller (Army); avionics 1750A microprocessor (USAF)

Honeywell. Radiation Hardened Static RAMs (Army, Navy, NASA); EMSP (Navy); MILSTAR (USAF)

Hughes. ATF common integrated processor (USAF); APG-65/70/71 radars (USAF, Navy); B-2 radar and upgrade (USAF); Advanced Special Receiver ALR-67 upgrade (Navy); LEAP (SDIO); AMRAAM processor and range correlator (USAF); MTSP (Army); LHX risk reduction program (Army); D3 fire control system (Army); UHF follow-on to LANDSAT (Navy); AUSSAT (Australian communications satellite); EHF satellite payload

IBM. Portable Jammer (Navy); Prism; SABIR (USAF); ISTP (NASA); ASW receiver (Navy)

Lockheed. Boost Surveillance and Tracking System (USAF); MILSTAR satellite payload (USAF)

Raytheon. Advanced onboard signal processing (AF/ARPA); advanced processor for air-to-air missiles (USAF); AEGIS standard missile (Navy); AIM-54C Phoenix missile (Navy); AMRAAM missile producibility enhancement (Navy/USAF); SLQ-32 electronic warfare system (Navy); CCS Mk-2 Command and control software for the BSY-1 submarine combat system (Navy); ground-based radar (Army); IR Maverick AGM-65D (USAF); MILSTAR (USAF); MILVAX (USAF); MK XV IFF (USAF); Patriot MCC Missile (Army); Sparrow Missile (Navy); Tartar Missile (Navy)

Texas Instruments. ATF (YF-22 version) mission display processor (USAF); target acquisition systems (Army); Space Station (NASA); LHX helicopter (Army); TOW 2 Auto Tracker (Army/ARPA); VETRONICS (Army); Anti-Armor Weapon System-Medium (Army); Short Range Attack Missile-II (USAF)

TRW. Radiation Hard 32-bit Computer (USAF); ICNIA (USAF); INEWS (USAF); Battle Management Processor (Army); Cryogenic CMOS for focal plane array (Navy); mass memory subsystem (USAF); advanced spacecraft computer module (USAF); advanced communications satellite processor (Navy); Standard EHF Package (USAF); ATF digital avionics (USAF)

UNISYS. V1750 Processor for various programs (IRAD); Radiation Hard 32-bit Processor (USAF/ SDIO)

Westinghouse. Combined FLIR and multifunction radar processor (Navy); Longbow signal processor for AH-64 helicopter (Army); ATF signal processor; ARSR-4 air route surveillance radar (FAA/USAF)

Logistics Retrofit Engineering. Numerous USAF electronic systems contain older devices that are fast becoming unavailable, while other components are unreliable, causing a significant degradation in operational availability. As a result, a number of VHSIC insertion projects have been undertaken by the service, in conjunction with the VHSIC Program Office, in which in-house facilities have been used to customize commercially

produced VHSIC gate arrays which can be tailored to perform the function(s) needed to replace no longer available chips. If needed, a "form, fit, function" replacement for an obsolete or unreliable part can be developed by creating a custom interconnect layer within the chip which determines the manner (i.e. logic) with which individual gates (transistor) within the array are interconnected. Examples of the work that has been accomplished within this area include replacement of an obsolete chip in the AJN-16 inertial navigation system and the APQ-130 radar onboard the F-111D aircraft, a new Weapon Navigation Computer board using VHSIC technology for the F-111; a VHSIC-based Communication Multiplexer for the Cheyenne Mountain Complex, and a VHSIC-like based modular system architecture for the FPS-117 3D surveillance radar.

Funding

Primary program funding was provided under US Air Force Program Element (PE) #0603452F, Very High Speed Integrated Circuits (VHSIC) RDT&E. This DoD program which concentrated on the initial development of VHSIC technology was completed in FY89. Funding for further VHSIC development has been assimilated by the various programs which now incorporate VHSIC technology in order to meet technical and/or cost objectives.

Analysis. Microelectronics have come to form the foundation of the international electronics industry. Even the US DoD Defense Critical Technologies Plan/DoD Defense Key Technologies Plan has placed a very significant, if not predominant, emphasis on electronics, specifically microelectronics and the area of Large Scale Integration. This, in turn, has called attention to the demand for the continuing development of semiconductor materials and microelectronic circuits. The net result has been the development of VHSIC technology and its subsequent infusion into production applications.

The VHSIC program has facilitated the development of products based on advanced semiconductor production technology by providing greatly accelerated component insertion rates. Following the successful completion of the VHSIC program, as marked by the large scale production of a broad spectrum of sophisticated microcircuit devices, ARPA and the services have directed their focus on the next generation of microcircuits (microwave and millimeter-wave monolithic integrated circuits — MIMIC) to provide affordable, reliable analog circuits for sensors and signal processors in military sensors, communications devices and munitions. Using the VHSIC program as a model, this program is now also reaching a successful conclusion and is being succeeded by the follow-on Microwave and Analog Front End Technology (MAFET) program being funded under DoD Program Element PE 0603739E. This project, initiated in 1995, has a continuous time line which extends into the 21st century and identifies a requested expenditure of more than US$-366 million by the year 2001. The stated objective of the MAFET program is to continue to pursue microcircuit cost reduction, enhance reliability and environmental performance and to continue to increase the functionality, and decease the size, of microcircuit chips. (See separate MIMIC report).

The VHSIC thrust has built a technological foundation that is being capitalized on in a wide range of current production applications. While VHSIC no longer exists as an independent program entity, its development is continuing under the auspices of the various new programs that are using the technology. However, there is still a significant problem to be resolved in reducing the cycle time it takes to field VHSIC into particular pieces of equipment. Ways to speed up this process are being aggressively studied, with significant progress being made.

A number of noteworthy accomplishments have been achieved through the VHSIC program. One big breakthrough is in the cost of designing silicon chips. Back in 1980 the cost to design a silicon chip was between US$100 and US$200 per gate, with the design of a 20,000 gate chip requiring an investment of some US$2 million over a period of at least two calendar years. A short decade later, in 1990, a two order-of-magnitude reduction in cost had been achiev ed, with a development lead time measured in months. VHSIC has further managed to leverage the significant advances of the US semiconductor industry which were initially developed for military applications. Partly as the result of the VHSIC program, half-micron semiconductor technology is on the verge of broad commercialization. Only ten years ago it was thought that this would not be possible until at least the turn of the century. This significant leap has been achieved by constantly shrinking the individual components on a chip which, in turn, has resulted in higher packing densities and faster clock rates. VHSIC technology has been responsible for the successful development of a series of low-cost commercial desktop supercomputers, with additional innovations being announced almost daily.

Recent Contracts

Contractor	Award ($ millions)	Date/Description
Control Data	5.8	Apr 1990 — Exercise of option for VHSIC AYK-14 modules and associated technical data for the AYK-14 Navy Standard Airborne Computer (N00019-86-C-0002)
McDonnell	34.3	Sep 1991 — Face value increase to an FFP contract
Douglas		for VHSIC central computer (F33657-89-C- 2000, P00035)
Control Data	13.4	Nov 1991 — Delivery order to provide 192 VPM-25 (VHSIC processor module), and 96 type-8 chassis (N00163-92-D-0001)
IBM	55.4	Mar 1992 — FVI to an FFP for 288 VHSIC Central Computers for the F-15 aircraft. Also includes purchase of Reliability Improvement Warranty program and reprocurement data (F09603-89-G-0039-0008)
CDI	5.2	Jul 1992 — Delivery order to provide 74 VHSIC processor modules and 37 type eight enclosures as components for the AN/AYK 14 Navy Standard Airborne Computer and to support the F/A-18 Hornet (N00163-92-D-0001)
CDI	12.6	Sep 1992 — Delivery order to provide 250 VHSIC processor modules supporting the Tactical Air Operations Module (N00163-92-D-0001)
IBM	8.3	Sep 1992 — FFP FVI for 43 VHSIC Central computers in support of War Readiness Material requirements for F-15A/B/C/D/E aircraft (F09603-89-G-0039-0009)
CDI	5.0	Dec 1992 — Delivery order to provide 72 VHSIC processor modules and 36 Type 8 chassis enclosure in support of the AYK-14 Navy Standard Airborne Computer to support F/A-18 Finland installs. This contract is 100 percent for Finland under the FMS program (N00163-92-D-0001)

Timetable

	1978	Program "kick-off" meeting
	1979	First VHSIC program director appointed; new VHSIC line items of US$12 million established in FY80 budget
Jun	1979	RFP issued for Phase 0 — Program Definition
Nov	1979	RFP issued for Phase 3
Mar	1980	Phase 0 contracts awarded
Jun	1980	Phase 3 contracts awarded
Sep	1980	RFP for Phase I issued
Dec	1980	Phase 0 completed
May	1981	Phase 1 contracts awarded
	1983	Fifteen weapon systems selected for Technology Insertion
Feb	1983	First fully functional VHSIC chip — TRW Matrix Switch
	1984	Yield Enhancement modifications to Phase 1 contract executed
May	1984	Acoustic signal processor using VHSIC chip demonstrated by IBM

Nov	1984	Phase 2 contracts awarded
	1985	Yield Enhancement and Manufacturing Technology programs started
Jul	1986	First system demonstration of VHSIC technology — ALQ-131 with Phase 1 chips; MIL-STD-1750A computer brassboard using VHSIC chips demonstrated
Dec	1986	Demonstration of VHSIC chip set in EPLRS
Dec	1987	VHSIC Hardware Description Language (VHDL) adopted for industry- wide design language as IEEE Standard 1076
Sep	1988	VHDL documentation mandated by DoD for all new systems
Nov	1988	Complex vector processor module for ATF demonstrated
Dec	1989	Demonstration of a fully functional CPUAX superchip running at 12 MHz
	1990	Specific VHSIC program element efforts completed
	1991	VHSIC technology placed into recipient programs
Dec	1991	VLSI of CPUAX superchip
Sep	1992	VHSIC processor modules ordered for US Navy Tactical Air Operations Modules. VHSIC chips installed in War Readiness computers
	1996	VHSIC integration into various electronic systems continues

Worldwide Distribution

VHSIC has fundamentally been a US program; however, some of the technology is starting to be installed in US military products sold overseas to selected allies. NATO members are also benefiting from the technology development and are now producing their own processors and other electronic equipment using VHSIC chips.

Forecast Rationale

The overall market for VHSIC technology will continue to maintain healthy growth throughout the forecast period, both in the US and abroad. We will continue to cover the expanding use of VHSIC technology, as well as associated developments, in this and related reports.

Due to a combination of the almost boundless opportunities for the application of VHSIC technology and the fact that the technology has reached a state of development such that the cost of individual circuit developments is increasingly being assimilated (and hidden) in end product development programs, it is difficult to assign a monetary value to the overall VHSIC technology development effort. We have provided a value forecast below for VHSIC technology development, but consider it to have a wide margin of uncertainty. During the last 12 years, it is estimated that approximately US$1 billion in funding has been committed to the VHSIC development program.

Ten-Year Outlook

FORECAST FUNDING LEVELS
(FY95 US $ Millions)

			High Confidence Level			Good Confidence Level				Speculative			
Designation	Application	thru 95	96	97	98	99	00	01	02	03	04	05	Total 96-05
VHSIC	SEMICONDUCTORS (DOD/USAF/USN/ USA)	1650.00	290.00	275.00	250.00	230.00	215.00	205.00	200.00	200.00	180.00	180.00	2225.00